DRAWINGS

The attached sheets of replacement drawings are submitted in compliance with 37 C.F.R. § 1.83(a), to replace the original sheets containing FIGs. 1 and 4 and correct anomalies. No new matter is added.

Attachment: two Replacement Sheets.

REMARKS

Claims 1-19 are pending in this application, of which claims 1, 8 and 15 are independent. Claim 19 is added without new matter. Support for new claim 19 is found at least in paragraph [0028]. For example, paragraph [0028] teaches "x and y-dimensions (e.g., see figures 5-10, 13) of the first circuit design 118 are therefore scaled differently."

Specification Objections

The specification stands objected to because of informalities. Paragraph [0031] is amended to correct a typographical error. For example, port instance 256 is described as being located at position X2, Y1, as shown in FIG. 4, and not X1, Y1. Paragraph [0032] is amended to correct a typographical error. For example, port instance 276 is described as being within cell layout 272, as shown in FIG. 4, and not within cell layout 172. Paragraph [0035] is twice amended to correct the name of element 122, to second circuit design 122, as shown in FIG. 1. No new matter is added.

Drawing Objections

The drawings stand objected to because of two informalities. Replacement drawing sheets are provided to correct FIGURE 1 and FIGURE 4. For example, in Figure 1, the label of item 120 is amended to read FIRST LAYOUT within computer memory 104 to match that of item 120 within storage device 106. In Figure 4, the text "W2" is added to the dimension beneath item 278 as supported by paragraph [0032]. No new matter is added.

Claim Rejections – 35 U.S.C. § 102

Paragraph 4 of the pending office action states that claims 1-4 and 6-17 stand rejected under 35 U.S.C. § 102(b) as being unpatentable over US Patent Number 5,936,868 to Hall (hereinafter "Hall"). However, no reason for rejection of claim 12 is provided. We therefore believe that only claims 1-4, 6-11 and 13-17 stand rejected under 35 U.S.C. § 102(b) as being unpatentable over Hall. Further clarification is requested. In view of the rejections to claims 1-4, 6-11 and 13-17, respectfully, we disagree.

As background, the immediate application teaches of asymmetrically shrinking a layout for a VLSI circuit design. As taught by paragraph [0028] of the specification and shown in figures 5-10 and 13, scaling of a first layout to generate a second layout is asymmetrical; x and y-dimensions of the first layout are scaled differently. In one example, a second design rule of a second fabrication process prohibits transistor rotation such that asymmetrical scaling is applied to allow for un-rotated transistors in the x-dimension while minimizing impact on performance and timing of signals traversing the y-dimension.

On the other hand, Hall discloses a method for converting an original integrated circuit (IC) design to an updated IC design for an updated manufacturing process; but Hall does not disclose or suggest asymmetrical scaling. That is, Hall does not disclose different x and y-dimension scaling factors. In the method of Hall, as noted by the Examiner, different scaling factors are applied to the original IC design; however, these 'different' scaling factors are applied at different times, and to different parts, during the shrinking of the original IC design. And Hall applies the same scaling factor to x and y-dimensions each time. See, e.g., Hall, col. 7, lines 3-6: "the original cell 20A, 20B and 20C (FIGS. 1A, 1B and 1C, respectively) is first scaled downward by a predetermined factor, such as 0.8, to produce the cell 22A, 22B and 22C (FIGS. 2A, 2B and 2C, respectively)." Hall continues: "the contacts 34 and vias 35 may also be scaled in separate steps when different scaling factors are desired." See Hall, col. 7, lines 17-20. Each scaling factor thus applies to a separate step. Hall does not specifically disclose different scaling factors for x and y-dimensions, and therefore cannot disclose asymmetrical scaling.

To anticipate a claim, Hall must teach every element of the claim and "the identical invention must be shown in as complete detail as contained in the ... claim." *MPEP 2131* citing *Verdegaal Bros. V. Union Oil Co. of California*, 814 F.2d 628, 2 USPQ2d 1051 (Fed. Cir. 1987) and *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 9 USPQ2d 1913 (Fed. Cir. 1989). Hall does not teach every element of claims 1-4, 6-11 and 13-17.

Claim 1 recites a process for asymmetrically shrinking a layout for a VLSI circuit design, including:

a) asymmetrically scaling a first VLSI circuit design layout defined by a first fabrication process, having first design rules, to a second VLSI circuit design layout defined by a second fabrication process, having second design rules; and

b) processing layouts of one or more leaf cells of the second VLSI circuit design layout to ensure conformity to the second design rules.

As noted above, Hall does not disclose or suggest asymmetrical scaling as required by element a) of claim 1. In col. 2, lines 1-14, as noted by the Examiner, Hall states "U.S. Patent number 5,018,174 to Griffith et al. (hereinafter "Griffith") discloses a method for making gate array masks in which a mask set for an existing set of gate array cells is converted to follow new design rules requiring non-uniform transformation of circuit components." Hall continues, col. 2 lines 9-12, "the patent takes advantage that for gate array cells, as compared to custom circuits, the masks/layout geometries differ only on the interconnect layers and the metal interconnect layers." Upon review of Griffith, however, no asymmetric scaling is applied. In fact, Griffith discloses manually converting the "most complex" cell manually from the old design rules to the new design rules, using a grid that spans the complex cell, and then applying the grid reference points to all other cells in the library. Thus, Griffith does not suggest a scaling process at all, but rather a re-layout process based upon a manually redefined grid.

Hall also does not specifically disclose or suggest that leaf cells of the second VLSI circuit design layout are processed to ensure conformity to the second design rules, as required by step b) of claim 1.

For at least these reasons, Hall cannot anticipate claim 1. Reconsideration of claim 1 is respectfully requested.

Claims 2-4, 6 and 7 depend from claim 1 and benefit from like argument. However, these claims have additional features that patentably distinguish over Hall. For example, claim 2 recites reorienting one or more transistors in accord with the second design rules. Hall does not disclose or suggest reorienting transistors and cannot anticipate claim 2. In paragraph 9 of the pending office action, the Examiner suggests that 'repositioning' within Hall is equivalent to 'reorienting' of the immediate application. Respectfully we disagree. Nowhere does Hall disclose or suggest transistor rotation; Hall only shows repositioning without rotation in FIGs. 1-5.

Claim 4 recites processing via arrays of the second VLSI circuit design layout to conform to the second design rules. As taught by paragraph [0049] of the specification, "layouts of one or more leaf cells (e.g., cell instances D1, D2, E1 and E2, figure 3) of the second VLSI circuit design layout are processed to ensure conformity to the second design rules (e.g., second design rules 132)." Figure 11 and paragraphs [0042-47] provides additional detail on this process. Although Hall does disclose "performing a third downward size scaling on the mask data to further downwardly scale the vias for the new or updated process," Hall does not specifically disclose processing of ***via arrays***, as required by claim 4.

Claim 7 recites maintaining locations of port instances relative to the asymmetric scaling between the first VLSI circuit design layout and the second VLSI circuit design layout. Hall does not perform asymmetric scaling, as required by claim 7.

For at least these reasons, Hall cannot anticipate claims 2-4, 6 and 7. Reconsideration of claims 2-4, 6 and 7 is respectfully requested.

Claim 8 recites a software product having instructions, stored on computer-readable media, wherein the instructions, when executed by a computer, perform steps for asymmetrically shrinking a layout for a VLSI circuit design, including:

a) instructions for asymmetrically scaling a first VLSI circuit design layout, defined by a first fabrication process having first design rules, to a second VLSI circuit design layout, defined by a second fabrication process having second design rules; and

b) instructions for processing layouts of one or more leaf cells of the second VLSI circuit design layout to ensure conformity to the second design rules.

Arguments presented for claim 1 also apply to claim 8. For example, Hall does not disclose asymmetrical scaling as required by step a) of claim 8 and Hall does not specifically disclose or suggest that leaf cells of the second VLSI circuit design layout are processed to ensure conformity to the second design rules, as required by step b) of claim 8. For at least these reasons, Hall cannot anticipate claim 8.

Reconsideration of claim 8 is respectfully requested.

Claims 9-11, 13 and 14 depend from claim 8 and benefit from like argument. However, these claims have additional features that patentably distinguish over Hall. For example, claim 9 recites reorienting one or more transistors in accord with the second design rules. As argued above with respect to claim 2, Hall does not disclose reorienting one or more transistors as required by claim 9. Claim 11 recites processing via arrays of the second VLSI circuit design layout to conform to the second design rules. As argued above with respect to claim 4, Hall does not specifically process via arrays as required by claim 11. Claim 14 recites maintaining locations of port instances relative to the asymmetric scaling between the first VLSI circuit design layout and the second VLSI circuit design layout. As argued above, since Hall does not disclose asymmetrical scaling, as required by claim 14.

For at least these reasons, Hall cannot anticipate claims 9-11, 13 and 14. Reconsideration of claims 9-11, 13 and 14 is respectfully requested.

Claim 15 recites a system for asymmetrically shrinking a layout for a VLSI circuit design, including:

a) means for asymmetrically scaling a first VLSI circuit design layout, defined by a first fabrication process having first design rules, to a second VLSI circuit design layout, defined by a second fabrication process having second design rules; and

b) means for processing layouts of one or more leaf cells of the second VLSI circuit design layout to ensure conformity to the second design rules.

Arguments presented above regarding claim 1 also apply to claim 15. For example, since Hall does not disclose asymmetrical scaling, hall cannot anticipate step a) of claim 15. Further, since Hall does not specifically disclose processing layouts of one or more leaf cells of the second VLSI circuit design, Hall cannot anticipate step b) of claim 15. For at least these reasons, Hall cannot anticipate claim 15.

Reconsideration of claim 15 is respectfully requested.

Claims 16 and 17 depend from claim 15 and benefit from like argument. However, these claims have additional features that patentably distinguish over Hall. For example, claim 16 recites a layout update tool. As shown in FIG. 12 of the drawings and taught by paragraph [0041] of the specification, layout update tool 116 includes a scale tool 502 that is "used to scale first layout 120 to a pitch associated with second fabrication process 128" and that "asymmetrical scaling factors for x and y-dimensions are made in step 402, for example, to accommodate transistor rotation limitations in the x-dimension." Hall does not disclose or suggest such a tool (nor asymmetric scaling) and therefore cannot anticipate claim 16. For at least these reasons, Hall cannot anticipate claims 16 and 17.

Reconsideration of claims 16 and 17 is respectfully requested.

Claim Rejections – 35 U.S.C. § 103

When applying 35 U.S.C. §103, the following tenets of patent law must be adhered to:

a) The claimed invention must be considered as a whole;

b) The references must be considered as a whole and must suggest the desirability and thus the obviousness of making the combination;

c) The references must be viewed without the benefit of impermissible hindsight vision afforded by the claimed invention; and

d) Reasonable expectation of success is the standard with which obviousness is determined. MPEP §2141.01, *Hodosh v. Block Drug Co., Inc.*, 786 F.2d 1136, 1134 n.5, 229 U.S.P.Q. 182, 187 n.5 (Fed. Cir. 1986).

In addition, it is respectfully noted that to substantiate a *prima facie* case of obviousness the initial burden rests with the Examiner who must fulfill three requirements. **First**, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the references or to combine reference teachings. **Second**, there must be a reasonable expectation of success. **Finally**, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicant's disclosure. (emphasis and formatting added) MPEP § 2143, *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Claims 5, 12 and 18 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Hall in view of U.S. Patent Number 6,756,242 granted to Regan (hereinafter "Regan"). Respectfully Applicants disagree.

Claim 5 depends from claim 1 and recites verifying hierarchy associated with the second VLSI circuit design layout. As argued above, Hall does not disclose all the subject matter of claim 1. For example, Hall does not disclose or suggest asymmetrical scaling as required by step a) of claim 1. Regan does not make up for the shortcomings of Hall, and therefore, even when combined, Hall and Regan cannot render claim 5 obvious.

Claim 12 depends from claim 8 and recites verifying hierarchy associated with the second VLSI circuit design layout. As argued above, Hall does not anticipate claim 8. Regan also does not have this disclosure, and, therefore, even when combined, Hall and Regan cannot render claim 12 obvious.

Claim 18 depends from claim 15 and recites verifying hierarchy associated with the second VLSI circuit design layout. As argued above, Hall does not disclose all the subject matter of claim 15. Further, Regan does not make up for the shortcomings of Hall, and therefore, even when combined, Hall and Regan cannot render claim 18 obvious.

Reconsideration of claims 5, 12 and 18 is respectfully requested.

New claim 19 depends from claim 1 and recites wherein the step of asymmetrically scaling simultaneously applies different x and y-dimension scaling factors. Neither Hall nor Regan disclose or suggest different x and y-dimension scaling factors as required by claim 19.

Applicants have addressed all issues raised in the Office Action dated August 5, 2005, and respectfully solicit a Notice of Allowance for claims 1-19. Applicants believe no fees are currently due, however, if any fee is deemed necessary in connection with this Amendment and Response, please charge Deposit Account No. 08-2025.

Respectfully submitted,

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